1. An integrated circuit manufacturing process for forming a floating gate device circuit in a surface of a silicon wafer, said process including the steps of:

providing a silicon substrate having a plurality of active device regions with gate dielectric thereon, a first central memory array portion of said silicon substrate containing active device regions having small feature size and a second peripheral control portion of said silicon substrate containing active device regions having large feature size, said active device regions being separated by isolation trenches filled with insulating material, said gate dielectric having a top surface, said insulating material filling said isolation trenches having a top surface, said top surface of said gate dielectric being recessed relative to said top surface of said insulating material filling said isolation trenches;

depositing a layer of polysilicon atop said top surface of said gate dielectric and said top surface of said insulating material filling said isolation trenches;

forming a protective mask over at least part of said second peripheral portion of said silicon substrate containing active device regions having large feature size;

polishing said layer of polysilicon to said top surface of said insulating material filling said isolation trenches in said first central portion of said silicon substrate using CMP, a first remaining portion of said layer of polysilicon remaining atop said gate dielectric in said first central portion of said silicon substrate, said first remaining portion of said layer of polysilicon forming self aligned polysilicon gates, a second remaining portion of said layer of polysilicon remaining in said at least part of said second peripheral portion of said silicon substrate;

said protective mask preventing substantial thinning of said polysilicon atop said active device regions having large feature size during said polishing step.

2. The process of claim 1, wherein said floating gate device circuit is a flash memory circuit.

3. The process of claim 2, further including the steps of:

depositing an ONO layer atop said top surface of said insulating material filling said isolation trenches and atop said first and second remaining portions of said polysilicon layer;

masking said first central portion of said silicon substrate;

etching away said ONO layer from said second peripheral portion of said silicon substrate; and

etching away said second remaining portion of said polysilicon layer.

4. The process of claim 2, wherein said small feature size comprises less than 3 micron dimension, and wherein said large feature size comprises greater than 3 micron dimension.

5. The process of claim 2, wherein said protective mask comprises silicon dioxide or silicon nitride.

6. The process of claim 5, wherein said protective mask has a thickness in the range between 30 and 300 Angstroms.

7. The process of claim 6, wherein said protective mask has a thickness in the range between 50 and 200 Angstroms.

8. The process of claim 2, wherein said active device regions in said second peripheral portion of said silicon substrate are patterned with a peripheral region of an active silicon mask, and wherein said protective mask is formed by the steps of:

depositing a protective layer atop said layer of polysilicon;

forming a shrunk said peripheral region of said active silicon mask by shrinking feature sizes on said peripheral region of said active silicon mask by a shrinking dimension;

patterning said protective layer with said shrunk said peripheral region of said active silicon mask; and

etching said patterned protective layer to form said protective mask.

9. The process of claim 8, wherein said shrinking dimension is in the range between 0.1 micron and 5 microns.

10. The process of claim 9, wherein said shrinking dimension is in the range between 0.3 and 1 micron.

11. The process of claim 2, wherein said protective mask is formed by the steps of:

providing a peripheral region mask covering substantially all of said second peripheral portion of said silicon substrate and having an opening window which leaves said first central portion of said silicon substrate uncovered;

patterning said protective layer with said peripheral region mask; and etching said patterned protective layer to form said protective mask.

12. The process of claim 11, wherein said opening window of said peripheral region mask is in the range between 5 and 30 microns larger than said first central portion of said silicon substrate.

13. A flash memory circuit made using the process of claim 1.

14. A flash memory circuit made using the process of claim 3.

15. A flash memory circuit made using the process of claim 8.

16. A flash memory circuit made using the process of claim 11.

17. An integrated circuit manufacturing flash memory intermediate product comprising:

a silicon substrate having a plurality of active device regions with gate dielectric thereon, a first central memory array portion of said silicon substrate covering 65 – 75 percent of the area of said silicon substrate containing active device regions having small feature size and a second peripheral control portion covering 25 – 35 percent of the area of said silicon substrate containing active device regions having large feature size, said active device regions being separated by isolation trenches filled with insulating material, said gate dielectric having a top surface, said insulating material filling said isolation trenches having a top surface, said top surface

of said gate dielectric being recessed relative to said top surface of said insulating material filling said isolation trenches;

a layer of polysilicon atop said top surface of said gate dielectric and said top surface of said insulating material filling said isolation trenches; and

a protective mask over at least part of said second peripheral portion of said silicon substrate containing active device regions having large feature size.

18. The integrated circuit manufacturing intermediate product of claim 17, wherein said at least part of said second peripheral portion of said silicon substrate containing active device regions having large feature size comprises said active regions having large feature size shrunk by a shrinking dimension.

19. The integrated circuit manufacturing intermediate product of claim 18, wherein said shrinking dimension is in the range between 0.3 and 1 micron.

20. The integrated circuit manufacturing intermediate product of claim 17, wherein said at least part of said second peripheral portion of said silicon substrate containing active device regions having large feature size comprises substantially all of said second peripheral portion of said silicon substrate and said protective mask having an opening window which leaves said first central portion of said silicon substrate uncovered.

21. The integrated circuit manufacturing intermediate product of claim 20 wherein said opening window of said protective mask is in the range

between 5 and 30 microns larger than said first central portion of said silicon substrate.